PISCES: A P4-Enabled OVS

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PISCES: A P4-Enabled OVS
Internal Architecture of OVS

OVS

DPDK
Internal Architecture of OVS
Internal Architecture of OVS
Internal Architecture of OVS
Internal Architecture of OVS
Road to Protocol Independence

Domain-Specific Language

Parser  Match-Action Pipeline

Compile

OVS

Parser  Match-Action Pipeline

DPDK
Road to Protocol Independence

P4 is an open-source language.\textsuperscript{[1]}

Describes different aspects of a packet processor:
- Packet headers and fields
- Metadata
- Parser
- Actions
- Match-Action Tables (MATs)
- Control Flow

\textsuperscript{[1]} http://www.p4.org
Road to Protocol Independence

P4 [1]

Parser → Match-Action Pipeline → Compile → Native OVS

OVS

Parser → Match-Action Pipeline

DPDK

341 lines of code

14,535 lines of code

Road to Protocol Independence

P4[1]

Compile

Performance Overhead!

OVS Forwarding Model

OVS

P4 Forwarding Model

http://www.p4.org

DPDK

P4 Forwarding Model (Post-Pipeline Editing)
OVS Forwarding Model

Ingress -> Packet Parser -> Match-Action Cache

Match-Action Tables

Egress

Flow Rule

Miss

Slow-path

Fast-path
OVS Forwarding Model
OVS Forwarding Model (Inline Editing)

[Diagram showing the OVS forwarding model with Ingress, Packet Parser, Match-Action Cache, and Egress paths.

- **Ingress**
- **Packet Parser**
- **Match-Action Cache**
- **Egress**

Pathways:
- **Slow-path**
- **Fast-path**
PISCES Forwarding Model (Modified OVS)

- Supports both editing modes:
  - Inline Editing
  - Post-pipeline Editing
PISCES: Compiling P4 to OVS
PISCES Forwarding Model (Modified OVS)
PISCES Forwarding Model (Modified OVS)

- Ingress Packet Parser
- Checksum Verify
- Microflow Cache
- Checksum Update
- Packet Deparser
- Egress

Match-Action Tables

Megaflow Cache

Slow-path

Fast-path
PISCES Forwarding Model (Modified OVS)
Naïve Compilation from P4 to OVS (L2L3-ACL)

Performance overhead of ~ 40%
Causes of Performance Overhead

CPU Cycles per Packet

Ingress
- Packet Parser
- Checksum Verify
- Megaflow Cache
- Checksum Update
- Packet Deparser
- Egress

Cache Misses

Match-Action Tables
Cause: CPU Cycles per Packet

L2L3-ACL (CPU Cycles for a 64 Byte Packet)

Throughput (Gbps)
Factors affecting CPU Cycles per Packet

a. Extra copy of headers
b. Fully-specified Checksum
c. Parsing unused header fields

and more ...
Different Optimizations for L2L3-ACL

L2L3-ACL (CPU Cycles for a 64 Byte Packet)

Throughput (Gbps)
Optimized Compilation from P4 to OVS (L2L3-ACL)

Performance overhead of < 2%
Cause: Cache Misses

- 3500+ Cycles (50x Cache hit)
- Throughput < 1 Mpps

Diagram:
- **Ingress**
  - Packet Parser
  - Checksum Verify
  - Match-Action Cache
  - Checksum Update
  - Packet Deparser
- **Egress**
Factors affecting Cache Misses

a. Entropy of packet header fields

b. Stateful operations in the match-action cache (or fast path).
PISCES Forwarding Model (Modified OVS)
PISCES Forwarding Model (Modified OVS)
Internals of the Microflow Cache

Packet in → Extract Fields → Hash Fields → Perform Lookup → Packet out

P4 File

to Megaflow Cache

Hit / Miss

Microflow Cache
Performance with the Microflow Cache

Phy-Phy, L3 Router Case, 64B

![Chart showing throughput comparison between OVS and PISCES. OVS has a throughput of 7.728 Gbps, while PISCES has a throughput of 6.464 Gbps.](image)
# Cause of Performance Degradation

<table>
<thead>
<tr>
<th>Cacheline</th>
<th>64 Bytes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Metadata</td>
</tr>
<tr>
<td>1</td>
<td>Metadata</td>
</tr>
<tr>
<td>2</td>
<td>IPv4 (1\textsuperscript{st} 16Bytes)</td>
</tr>
</tbody>
</table>

**Simplified “flow” Structure**
Performance with the Microflow Cache

Phy-Phy, L3 Router Case, 64B

Throughput (Gbps)

7.728  8.198

OVS  PISCES
Varying the Number of Hash Fields

Throughput (Gbps)

- L2 Address (2 Fields): 8.682 Gbps
- Five Tuple (5 Fields): 8.198 Gbps
Questions?
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